SEMICONDUCTOR DEVICE HAVING HIGH BREAKDOWN VOLTAGE

This is a division of application Ser. No. 603,976, filed Oct. 23, 1990.

BACKGROUND OF THE INVENTION

This invention relates to a semiconductor device and to a method of manufacturing a semiconductor device.

U.S. Pat. No. 4,003,072 describes a semiconductor device comprising a semiconductor body having a first device region of one conductivity type forming with a second device region of the opposite conductivity type provided adjacent one of the major surfaces of the semiconductor body a first pn junction which is reverse-biassed in at least one mode of operation of the device, and a floating further region of the opposite conductivity type provided within the first device region remote from the major surfaces of the semiconductor body and spaced from the second device region so that, in the one mode of operation of the device, the depletion region of the first pn junction reaches the floating further region before the first pn junction breaks down.

Such a device is shown in, for example, FIG. 5 of U.S. Pat. No. 4,003,072 where an array of floating further regions is provided. The floating further regions act to increase the voltage at which the device breaks down when the first pn junction is reverse-biassed in operation of the device. Thus, when under such reverse-biassing conditions the first region is depleted of free charge carriers, the ionized impurity atoms in the further floating regions act to divert electric field lines from the oppositely charged ionized impurity atoms in the first device region. These electric field lines would otherwise serve to increase the field at the first pn junction and help to cause breakdown at the first pn junction. However, because of the tendency of the pn junction(s) between the floating further region(s) and the first device region to become forward-biassed, which reduces the potential between the second device region and the floating region and may cause the potential of the floating region to become fixed, it is difficult for high electric fields to exist above the floating further region(s). This adversely affects the reverse breakdown voltages which can be attained.

SUMMARY OF THE INVENTION

It is an aim of the present invention to provide a semiconductor device and a method of manufacturing such a semiconductor device which overcomes or at least mitigates the above-mentioned problems, enabling even higher breakdown voltages to be achieved.

According to one aspect of the present invention, there is provided a semiconductor device comprising a semiconductor body having a first device region of one conductivity type forming with a second device region of the opposite conductivity type provided adjacent one of the major surfaces of the semiconductor body a first pn junction which is reverse-biassed in at least one mode of operation of the device, and a floating further region of the opposite conductivity type provided within the first device region remote from the major surfaces of the semiconductor body and spaced from the second device region so that, in the one mode of operation of the device, the depletion region of the first pn junction reaches the floating further region before the first pn junction breaks down, characterized in that the further region forms a further pn junction with a highly doped capping region of the one conductivity type provided within the first device region between the floating further region and the second region and spaced from the second region.

In another aspect, the present invention provides a method of manufacturing a semiconductor device, which method comprises providing a first semiconductor body part having a first region of one conductivity type adjacent one surface, providing a further region of the opposite conductivity type adjacent the one surface within the first body part, providing a second semiconductor body part on the one surface to form with the first body part a semiconductor body having opposed major surfaces and to provide a second region of the one conductivity type on the one surface to form with the first region a first device region within which the further region is floating, and providing adjacent one major surface of the semiconductor body a second device region of the opposite conductivity type forming with the first device region a first pn junction which is spaced from the floating further region so that, when the first pn junction is reverse-biassed in at least one mode of operation of the device, the depletion region of the first pn junction reaches the floating further region before the first pn junction breaks down, characterized by providing adjacent the one surface a highly doped region of the one conductivity type which forms a further pn junction with the further region and provides a capping region between the further region and the second device region spaced from the second device region.

Thus, in a semiconductor device embodying the invention, the floating region is capped by a highly doped region of the one conductivity type which enables a high electric field to exist between the first pn junction and the further floating region without the risk (or with less of a risk) of the pn junction formed by the further floating region with the first device region becoming forward-biassed which enables higher breakdown voltages to be achieved for a given resistivity of the semiconductor body.

Normally, if a single floating further region is provided it should be of comparable extent to the first pn junction. However, an array of floating further regions may be provided with each further region forming a further pn junction with a respective highly doped capping region of the one conductivity type provided within the first device region, the floating further regions being equally spaced from the first pn junction and being spaced from one another by a distance sufficient to avoid merging of the depletion regions associated with the further regions under zero bias. The provision of an array of further regions should allow, in comparison to the use of a single floating further region, a larger area for current flow between the major surfaces of the device which should lessen the possibility of current-crowding problems, especially where the semiconductor device is a vertical device with the main current path extending between the major surfaces. The device may be a bipolar transistor, in which case a third device region of the one conductivity type may be provided within the second device region. In the case of a bipolar transistor, the first device region may form at least part of the collector region of the transistor while the second and third device regions form the base and emitter regions, respectively.